MONOLITHIC MBE GaAs PIN DIODE LIMITER

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ABSTRACT

A broadband MBE GaAs PIN/NIP diode limiter has demonstrated 15 dB of isolation with a +32.5 dBm input signal while maintaining less than 0.25 dB of small-signal insertion loss from 0.05 GHz to 14 GHz. These results were obtained by incorporating vertical GaAs PIN/NIP diodes in a shunt-loaded microstrip configuration.

INTRODUCTION

Conventional radar receivers use hybrid Si PIN diode limiters to prevent transmitter power from burning out sensitive receiver components such as LNAs or mixers. To meet the required limiting and insertion loss specifications, the Si PIN diodes used in these limiters are extremely small, making them difficult to bond into circuits. The parasitic bond wire inductances used to connect the diodes into the circuit reduce the bandwidth over which the limiter maintains an acceptable small-signal match. A monolithic MBE GaAs PIN diode limiter has been developed that utilizes a combination of microstrip and vertical shunt-loaded PIN diodes to achieve less than 0.2 dB small-signal insertion loss and greater than 15 dB limiting at 10 GHz. The process used to fabricate the limiter is potentially compatible with FET circuits, allowing integration of other MMICs on the same substrate for future single-chip radar front ends. A number of these limiters have been fabricated and RF tested. The fabrication will be discussed as well as methods to increase limiting to greater than 15 dB.

GaAs PIN DIODE FABRICATION

The vertical PIN diode is fabricated on MBE grown layers as shown in Figure 1-A. The N+ layer and its doping transition from the substrate is grown so that FETs can be integrated with the PIN diodes. FETs can be integrated by addition of an E-beam masking step and suitable gate metal deposition. The fabrication process for the PIN diode, as outlined in Figure 1, begins with deposition and patterning of Au/Zn/Au for the P+ contact (Figure 1-A). The P+ is alloyed for 1 minute at 370°C. The mesa for the PIN diode is etched using the Au/Zn/Au as a mask (Figure

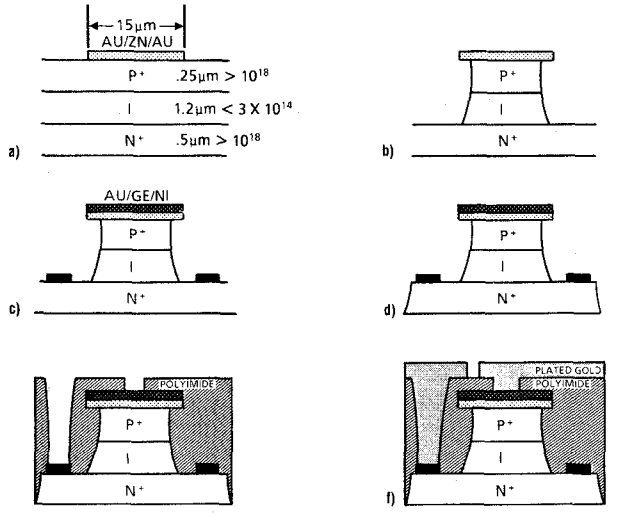

Figure 1. GaAs Monolithic MBE PIN Diode Fabrication

1-B). The GaAs is etched to the I/N+ interface (Figure 1-C). Au/Ge/Ni is deposited and patterned to form the contacts for the N+. The Au/Ge/Ni is self-aligned to the Au/Zn/Au and the P+ mesa. The Au/Ge/Ni is alloyed at 430°C for 3 minutes (Figure 1-D). At this point if an FET is desired, the gate can be patterned, recessed, and deposited. After the contact metals are alloyed, polyimide is spun onto the slice to form a dielectric crossover for the mesa (Figure 1-E). After the polyimide is patterned and cured, Ti/Au is deposited, patterned, and plated to form interconnects and transmission lines (Figure 1-F).

PERFORMANCE

To date, a number of PIN diodes have been fabricated and tested. A detailed plot of the forward characteristics of a PIN diode with an 18-μm diameter mesa is shown in Figure 2. The saturation current is approximately 100 fA. The IV curve shows no excess current at low fields and has an ideality factor of 2 from 10 pA to 1 mA. This represents the high quality junction grown by the MBE reactor and the absence of surface effects found in lateral structures. Also shown in Figure 2 is the incremental resistance of the PIN

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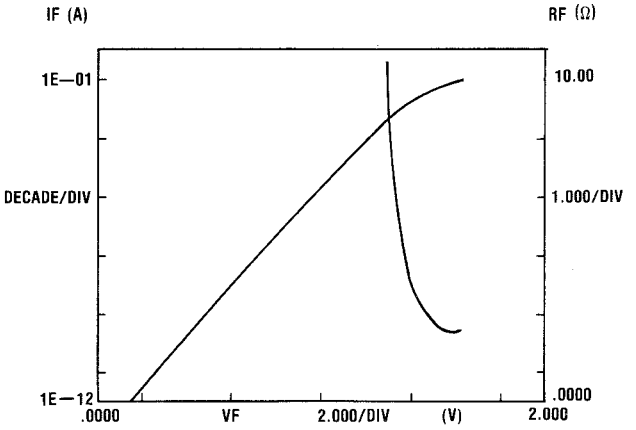

Figure 2. PIN Diode Forward I/V Characteristics

diode. This indicates that the parasitic resistance is less than 2 ohms. The reverse voltage-current characteristic is shown in Figure 3. The leakage current is less than 100 pA at 20 volts. The breakdown voltage is in excess of 40 volts at 10 uA. The storage time (Figure 4) measured with a 50-ps rise-time is approximately 2 ns. This places the lower frequency limit at 80 MHz.

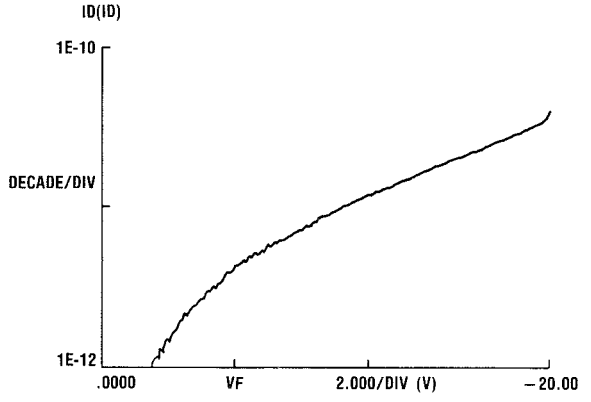

Figure 3. PIN Diode Reverse I/V Characteristics

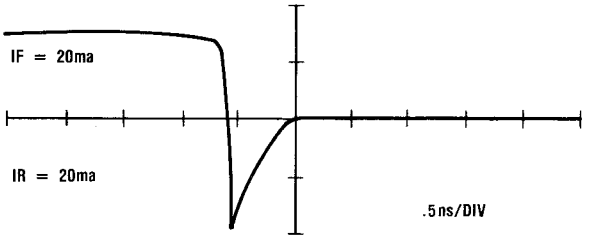

Figure 4. PIN Diode Storage Time

LIMITER DESIGN

A section of microstrip with the shunt-loaded PIN diodes is shown in Figure 5. Two vertical PIN diodes are incorporated in a PIN/NIP shunt configuration between a short section of 50-ohm microstrip line and ground. Via holes are used to provide low impedance paths to ground. The off capacitance of the PIN diode is 0.09 pF yielding a 3-dB bandwidth in a 50 ohm system in excess of 35 GHz. With 0.2 nH of bondwire at the input and output, SCOMPACT predicts an insertion loss of less than 0.25 dB through 14 GHz and a VSWR less than 1.5:1. The 50-ohm microstrip line serves as a transition between other components and also provides sufficient area for automated assembly and bonding. The measured small-signal insertion loss and the power limiting data are shown in Figures 6 and 7.

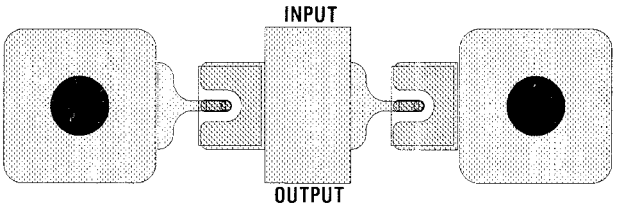

Figure 5. Monolithic MBE PIN / NIP Limiter Layout

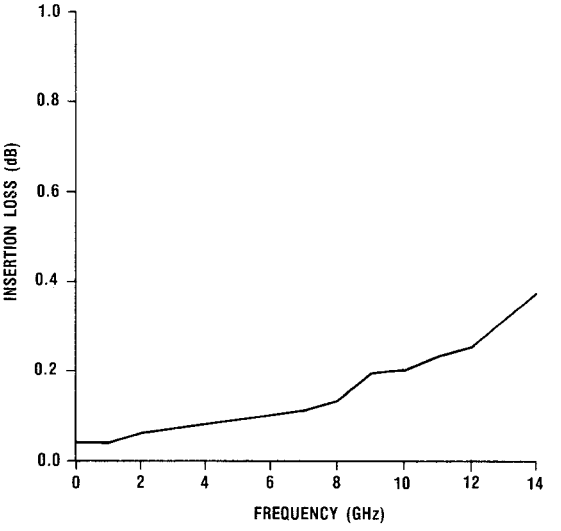

Figure 6. MBE Limiter: Small Signal Insertion Loss

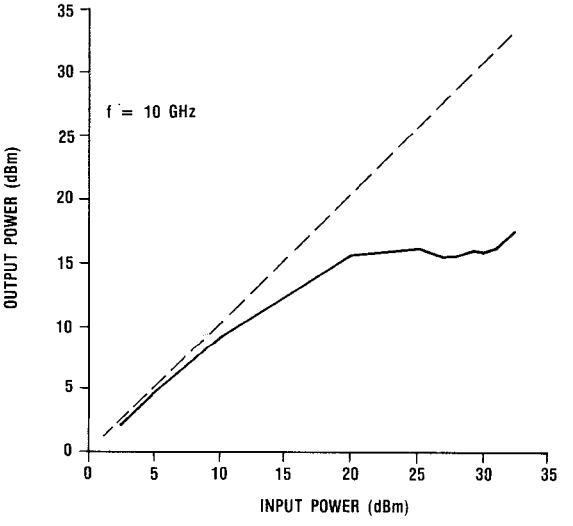

Figure 7. MBE Limiter: Large Signal Insertion Loss

CONCLUSION AND RECOMMENDATIONS

The vertical GaAs PIN diode has demonstrated the capability to limit power in monolithic form over broad bandwidths while maintaining low insertion loss at small-signal levels. Integration of the PIN limiter with the LNA to form a single-chip receiver will further enhance the performance of the receiver by removing the bondwire presently required to connect the two circuits.

ACKNOWLEDGEMENTS

The authors would like to express their gratitude to H. D. Shih for the MBE work and S. Duncan for her processing and evaluation of the PIN diodes.

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